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EXAMINER
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4144	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/573,250	HILL ET AL.	
	Examiner	Art Unit	
	BENJAMIN ELLIOTT	4144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) *63-67* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,24-62,68 and 69* is/are rejected.

7)☒ Claim(s) *15-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/23/2006, 1/19/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-69 have been examined and are pending. Of these, Claims 63-67 have been cancelled.

Information Disclosure Statement

2. Initialed and dated copies of the Applicant's form 1449 submitted on 3/23/2006 and 01/19/2007 are attached to the instant office action.

Claim Objections

3. Claim 61 is objected to because of the following informalities: the term "including the channel assignment process including the switching…". The sentence is grammatically incorrect and appropriate correction is required.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 57-60 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. With regards to the wording of the claims, "a suite of computer programs arranged to implement...", as described is non-statutory. The "programs" are not tied to tangible computer storage medium executed by a

machine or processor to provide necessary functional and structural interrelationship and to produce useful, concrete and tangible result(s).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-5, 7, 24, and 61 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 7,356,025 B2 by Bohm (hereinafter "Bohm").

As per Claim 1, Bohm discloses **a channel assignment process for a switch arrangement, the switch arrangement being arranged to perform the switching of traffic in both the space and time domains** (Col.3, lines 10-12. An object of the invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.), **the process comprising:**

receiving traffic along a number of ingress subelements of the switch (Col. 3, lines 20-21. Incoming bit streams are received at input ports. Figure 1; col. 10, lines 12-24.

Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

for each ingress aggregation comprising a subset of said plurality of ingress subelements (Col. 3, lines 15-19. The multistage switch comprises a number of switching elements that are arranged in stages. Each element contains a number of input ports.), **aggregating one or more time-slots of the ingress subelements comprising said ingress aggregation to form one or more aggregated time-space channels** (Col. 8, lines 50-53. Channel data of different time slots, but pertaining to the same channel may be switched via different paths.);

assigning one or more inner time-space channels (Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to "inner time-space channels" are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.) **available through at least one inner time-shared spatial switching stage of the switch arrangement to each aggregated time-space channel** (Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.); **and**

assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned through said at least one inner time-shared spatial switching stage (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage.).

As per Claim 2, Bohm discloses **a channel assignment process as claimed in claim 1, wherein each ingress aggregation further comprises a one or more switching stages forming a switching sub-structure of the switch arrangement** (Col. 3, lines 15-22. The multipath multistage switch comprises a number of switching elements, wherein each switching element comprises a plurality of inputs and outputs.).

As per Claim 3, Bohm discloses **a channel assignment process as claimed in claim 1, wherein said switch arrangement further comprises a plurality of egress aggregations, each egress aggregation comprising a subset of the egress subelements of the switch arrangement and one or more switching stages forming a switching sub-structure of the switch arrangement, wherein for each egress aggregation, one or more time-slots of the egress subelements are aggregated to form one or more aggregated time-space channels** (Col. 3, lines 15-

22. The multipath multistage switch comprises a number of switching elements, wherein each switching element comprises a plurality of inputs and outputs. Col. 8, lines 50-53. Channel data of different time slots, but pertaining to the same channel may be switched via different paths. Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage.).

As per Claim 4, Bohm discloses **a channel assignment process as claimed in claim 2, wherein at least one switching stage comprises a time-domain switching stage** (Col. 3, lines 15-19. The multistage switch comprises a number of switching elements that are arranged in stages. Each switching element provides for time and space switching.).

As per Claim 5, Bohm discloses **a channel assignment process as claimed in claim 3, wherein in said step of assigning a plurality of end-to-end channels, traffic received at an ingress subelement is assigned to an end-to-end channel comprising:**

at least one channel through an ingress aggregation;

at least one channel through each of the at least one inner time-shared spatial switching stages of the switch arrangement;

and at least one channel through an egress aggregation (Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to "inner time-space channels" are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.).

As per Claim 7, Bohm discloses **a channel assignment process as claimed in claim 1, in which the channel assignment process is implemented as a frame-based channel assignment process** (Col. 4, lines 64-67; col. 5, lines 1-3. Data is passed through channels in frames.).

As per Claim 24, Bohm discloses **a scheduling process for a switch arrangement, the switch arrangement being arranged to perform the switching of traffic in both the space and time domains** (Col.3, lines 10-12. An object of the invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.), **the process comprising:**

receiving traffic along a number of ingress subelements of the switch (Col. 3, lines 20-21. Incoming bit streams are received at input ports. Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contains three input ports and three output ports. These ports

correspond to "subelements" of applicant's invention.);

matching traffic at an ingress subelement of the switch to one or more available egress subelements of the switch (col. 3, lines 29-34. A channel is established between an input and an output based on bandwidth.);

and assigning channels to matched traffic by performing the steps of:

receiving traffic along a number of ingress subelements of the switch (Col. 3, lines 20-21. Incoming bit streams are received at input ports. Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

aggregating one or more time-slots from each of said plurality of ingress subelements to form a plurality of time-space channels which are aggregated by an aggregation of the said plurality of ingress subelements (Col. 3, lines 15-19. The multistage switch comprises a number of switching elements that are arranged in stages. Each element contains a number of input ports. Col. 13, lines 25-45. At the intermediate stage, it is sufficient to find a switching element that has enough available time slots of an incoming bit stream to carry a channel through enough available time slots of an outgoing bit stream to at least two switching elements, as this pertains to multicast of channels.);

assigning inner time-space channels available through at least one inner time shared spatial switching stage of the switch arrangement to said plurality of aggregated time-space channels (Col. 18, lines 3-13; Figure 1 and 6. The

intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.);

and assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned for switching through the said at least one inner time-shared spatial switching stage (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage.).

As per Claim 61, Bohm discloses **a scheduling process as claimed in claim 24, including the channel assignment process including the switching of traffic in both the space and time domains** (Col.3, lines 10-12. An object of the invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.), **said process comprising: receiving traffic along a number of ingress subelements of the switch** (Col. 3, lines 20-21. Incoming bit streams are received at input ports. Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contains three input ports and three output ports. These ports

correspond to “subelements” of applicant’s invention.);

for each ingress aggregation comprising a subset of said plurality of ingress subelements (Col. 3, lines 15-19. The multistage switch comprises a number of switching elements that are arranged in stages. Each element contains a number of input ports.), **aggregating one or more time-slots of the ingress subelements comprising said ingress aggregation to form one or more aggregated time-space channels** (Col. 8, lines 50-53. Channel data of different time slots, but pertaining to the same channel may be switched via different paths.);

assigning one or more inner time-space channels (Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.) **available through at least one inner time-shared spatial switching stage of the switch arrangement to each aggregated time-space channel** (Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.);

and assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch

arrangement after said aggregated channels have been assigned through said at least one inner time-shared spatial switching stage (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage.).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 6, 8, 9, 25-32, 35-38, 40-43, 49, 50, 55, 56, 62, 68, and 69 rejected under 35 U.S.C. 103(a) as being unpatentable over Bohm, and further in view of US Patent 6,343,075 B1 by Klausmeier et al (hereinafter "Klausmeier").

As per Claim 6 and 25, Bohm is silent on **a channel assignment (and scheduling) process for a switch arrangement as claimed in claim 1 (and 24), wherein the number of time-space inner channels provided by the logical switches of each of said at least one inner time-shared spatial switching stage of the switch arrangement to each ingress aggregation is equal to at least the number of time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an ingress aggregation.**

However, Klausmeier teaches the switches are of a logical arrangement and the logical switches of each of said at least one inner time-shared spatial switching stage of the switch arrangement to each ingress aggregation is equal to at least the number of

time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an ingress aggregation (Col. 5, lines 13-22. The center stage of the switch consists of a number of logically sub-divided sub-switches that are equal to the number of sub-frames. In the example given for the invention, the number of center stage switches is equal to 22, and the number of sub-switches is equal to 3. When these numerical values of center switches (elements) are multiplied by the number of sub-frames (subelements), the number of logical center stage sub-switches (inner time-shared spatial switches) becomes 66. Each sub-frame contains six time slots (Col. 4, lines 49-51). In the example given for the invention, working with the number of inputs (=384), the total number of center switching stages is 384/18 (outputs; this number is three sub-frames containing six time slots, 3 times 6 equals 18) equals 22.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include a middle switching stage comprising a plurality of logical switches, and the middle switch is used to provide a channel between the inputs and outputs taught by Klausmeier, wherein the middle switch can be logically reconfigured to consume less power and occupy less space (Col. 6, lines 9-14).

As per Claim 8, Bohm discloses **a channel assignment process as claimed in claim 1, in which said process is further iteratively performed within each ingress aggregation to determine a plurality of end-to-end channels through said ingress aggregation** (Col. 7, lines 27-38. The method comprises a switching apparatus that

contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.), wherein said inner channels comprise time-space channels provided by the logical switches of at least one inner time-shared spatial switching stage of the ingress aggregation element (Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.).

Bohm is silent on the switching elements having a “logical” configuration.

However, Klausmeier teaches a switching element is arranged or factored logically into sub-arrays of sub-elements or switching stages (Figure 4a; Col. 3, lines 46-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include logical switching arrangements to consume less power and occupy less space (Col. 6, lines 9-14).

As per Claim 9, Bohm discloses **a channel assignment process as claimed in claim 3, in which said process is further iteratively performed within each egress aggregation to determine a plurality of end-to-end channels through each said egress aggregation element, wherein said inner channels comprise time-space**

channels provided by the logical switches of at least one inner time-shared spatial switching stage of the egress aggregation element (Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to "inner time-space channels" are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.), wherein said inner channels comprise time-space channels provided by the logical switches of at least one inner time-shared spatial switching stage of the ingress aggregation element (Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.).

Bohm is silent on the switching elements having a "logical" configuration.

However, Klausmeier teaches a switching element is arranged or factored logically into sub-arrays of sub-elements or switching stages (Figure 4a; Col. 3, lines 46-56).

Examiner maintains motivation to combine the teachings of Bohm to include the teachings of Klausmeier as disclosed in Claim 8.

As per Claim 26, Bohm is silent on **a scheduling process as claimed in claim 24, wherein the number of time-space inner channels provided by the logical switches of each of said at least one inner time-shared spatial switching stage of**

the switch arrangement to each aggregation element is equal to at least the number of time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an aggregation element.

However, Klausmeier teaches the switches are of a logical arrangement and the logical switches of each of said at least one inner time-shared spatial switching stage of the switch arrangement to each ingress aggregation is equal to at least the number of time-slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an ingress aggregation (Col. 5, lines 13-22. The center stage of the switch consists of a number of logically sub-divided sub-switches that are equal to the number of sub-frames. In the example given for the invention, the number of center stage switches is equal to 22, and the number of sub-switches is equal to 3. When these numerical values of center switches (elements) are multiplied by the number of sub-frames (subelements), the number of logical center stage sub-switches (inner time-shared spatial switches) becomes 66. Each sub-frame contains six time slots (Col. 4, lines 49-51). In the example given for the invention, working with the number of inputs (=384), the total number of center switching stages is 384/18 (outputs; this number is three sub-frames containing six time slots, 3 times 6 equals 18) equals 22.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include a middle switching stage comprising a plurality of logical switches, and the middle switch is used to provide

a channel between the inputs and outputs taught by Klausmeier, wherein the middle switch can be logically reconfigured to consume less power and occupy less space (Col. 6, lines 9-14).

As per Claim 27, Bohm discloses **a switching process as claimed in claim 26, in which traffic received by an ingress subelement is switched at least once in the time-domain within an ingress aggregation comprising said ingress subelement before being switched spatially by at least one inner time-shared spatial switching stage of the switch arrangement** (Col. 4, lines 51-59. The first and last stages provide for time and space switching, while the intermediate stage provides for space switching.).

As per Claim 62, the combination of Bohm and Klausmeier discloses **a switching process according to claim 26, in which traffic is scheduled through a switch arrangement which switches traffic in both the space and time domains** (Bohm; Col.3, lines 10-12. An object of the invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.) **and comprises:**

a plurality of ingress subelements (Bohm; Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

a plurality of egress subelements (Bohm; Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120)

that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

means to receive traffic along said number of ingress subelements (Bohm; Col. 3, lines 25-28. The multipath switch of the invention contains a control unit for controlling the switching elements.);

means to store said received traffic (Bohm; Figure 2; col. 11, lines 6-13. A medium access unit (21-23) contains a buffer to store frames received from the bit stream.);

means to aggregate one or more time-slots from each of said plurality of ingress subelements to form a plurality of time-space channels which are aggregated for an ingress aggregation of the said plurality of ingress subelements (Bohm; Col. 11, lines 21-24. Time slot data from time slots of a frame are written into time slot data fields of a respective memory page.);

and at least one inner time-shared spatial switching stage, comprising a plurality of logical switches (Klausmeier; Col. 4, lines 58-61. The switching arrangement of the invention, wherein the center stage contains switches for time switching, the center stage may also contain additional switches that are logically created. Each of the center stage switches logically receives an 18-byte-wide bus (Col. 4, lines 65-67 and col. 4, lines 1-2). Klausmeier further teaches the center stage switching arrangement is logically created through a combination of time division and space switching (Col. 3, lines 41-44)), **wherein said plurality of logical switches are arranged to provide a number of time-space inner channels to each aggregation element which is equal to at least the number of time- slots that each ingress subelement switches end**

to end through the switch arrangement multiplied by the number of ingress subelements which form an aggregation element (Klausmeier; Col. 5, lines 13-22. The center stage of the switch consists of a number of logically sub-divided sub-switches that are equal to the number of sub-frames. In the example given for the invention, the number of center stage switches is equal to 22, and the number of sub-switches is equal to 3. When these numerical values of center switches (elements) are multiplied by the number of sub-frames (subelements), the number of logical center stage sub-switches (inner time-shared spatial switches) becomes 66. Each sub-frame contains six time slots (Col. 4, lines 49-51). In the example given for the invention, working with the number of inputs (=384), the total number of center switching stages is 384/18 (outputs; this number is three sub-frames containing six time slots, 3 times 6 equals 18) equals 22.)**;**

and switch processor means arranged to switch traffic received by the switch arrangement along a plurality of assigned end-to-end channels from the ingress subelements to the egress subelements (Bohm; Col. 3, lines 25-28. The multipath switch of the invention contains a control unit for controlling the switching elements.).

wherein a scheduling process is implemented to provide a channel assignment comprising:

receiving traffic along a number of ingress subelements of the switch (Bohm; Col. 3, lines 20-21. Incoming bit streams are received at input ports. Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports

correspond to “subelements” of applicant’s invention.);

for each ingress aggregation comprising a subset of said plurality of ingress subelements (Bohm; Col. 3, lines 15-19. The multistage switch comprises a number of switching elements that are arranged in stages. Each element contains a number of input ports.)**, aggregating one or more time-slots of the ingress subelements comprising said ingress aggregation to form one or more aggregated time-space channels** (Bohm; Col. 8, lines 50-53. Channel data of different time slots, but pertaining to the same channel may be switched via different paths.)**;**

assigning one or more inner time-space channels (Bohm; Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.) **available through at least one inner time-shared spatial switching stage of the switch arrangement to each aggregated time-space channel** (Bohm; Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.)**;**

and assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch

arrangement after said aggregated channels have been assigned through said at least one inner time-shared spatial switching stage (Bohm; Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage.).

Examiner maintains motivation to combine the teachings of Bohm to include the teachings of Klausmeier as disclosed in Claim 26.

As per Claim 28, Bohm discloses **a switch arrangement arranged to perform the switching of traffic in both the space and time domains** (Col.3, lines 10-12. An object of the invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.), **the switch arrangement comprising:**

a plurality of ingress subelements (Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

a plurality of egress subelements (Figure 1; col. 10, lines 12-24. Figure 1 shows three

stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

means to receive traffic along said number of ingress subelements (Col. 3, lines 25-28. The multipath switch of the invention contains a control unit for controlling the switching elements.);

means to store said received traffic (Figure 2; col. 11, lines 6-13. A medium access unit (21-23) contains a buffer to store frames received from the bit stream.);

means to aggregate one or more time-slots from each of said plurality of ingress subelements to form a plurality of time-space channels which are aggregated for ingress aggregation of the said plurality of ingress subelements (Col. 11, lines 21-24. Time slot data from time slots of a frame are written into time slot data fields of a respective memory page.);

and at least one inner time-shared spatial switching stage, comprising a plurality of logical switches, wherein said plurality of logical switches are arranged to provide a number of time-space inner channels to each aggregation element which is equal to at least the number of time- slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an aggregation element;

and switch processor means arranged to switch traffic received by the switch arrangement along a plurality of assigned end-to-end channels from the ingress

subelements to the egress subelements (Col. 3, lines 25-28. The multipath switch of the invention contains a control unit for controlling the switching elements.).

Bohm is silent on the middle switching stage comprising a plurality of logical switches, and the middle switch is used to provide a channel between the inputs and outputs.

However, Klausmeier teaches the switching arrangement of the invention, wherein the center stage contains switches for time switching, the center stage may also contain additional switches that are logically created (Col. 4, lines 58-61). Each of the center stage switches logically receives an 18-byte-wide bus (Col. 4, lines 65-67 and col. 4, lines 1-2). Klausmeier further teaches the center stage switching arrangement is logically created through a combination of time division and space switching (Col. 3, lines 41-44).

With regards to the following limitation, Klausmeier discloses **wherein said plurality of logical switches are arranged to provide a number of time-space inner channels to each aggregation element which is equal to at least the number of time- slots that each ingress subelement switches end to end through the switch arrangement multiplied by the number of ingress subelements which form an aggregation element** (Col. 5, lines 13-22. The center stage of the switch consists of a number of logically sub-divided sub-switches that are equal to the number of sub-frames. In the example given for the invention, the number of center stage switches is equal to 22, and the number of sub-switches is equal to 3. When these numerical values of center switches (elements) are multiplied by the number of sub-frames

(subelements), the number of logical center stage sub-switches (inner time-shared spatial switches) becomes 66. Each sub-frame contains six time slots (Col. 4, lines 49-51). In the example given for the invention, working with the number of inputs (=384), the total number of center switching stages is 384/18 (outputs; this number is three sub-frames containing six time slots, 3 times 6 equals 18) equals 22.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include a middle switching stage comprising a plurality of logical switches, and the middle switch is used to provide a channel between the inputs and outputs taught by Klausmeier, wherein the middle switch can be logically reconfigured to consume less power and occupy less space (Col. 6, lines 9-14).

As per Claim 29, Bohm discloses **a switch arrangement as claimed in claim 28, in which traffic received by an ingress subelement is switched at least once in the time-domain within an ingress aggregation comprising said ingress subelement before being switched spatially by at least one inner time-shared spatial switching stage of the switch arrangement** (Col. 4, lines 51-59. The first and last stages provide for time and space switching, while the intermediate stage provides for space switching.).

As per Claim 30, Bohm **discloses a switch arrangement as claimed in claim 28, further comprising:**

means to assign inner time-space channels available through at least one inner time-shared spatial switching stage of the switch arrangement to said plurality of

aggregated time-space channels (Col. 3, lines 25-28. The multipath switch of the invention contains a control unit for controlling the switching elements.); **and means to assign a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned for switching through the said at least one inner time-shared spatial switching stage** (Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contain three input ports and three output ports. These ports correspond to "subelements" of applicant's invention. Figure 2; col. 11, lines 6-13. A medium access unit (21-23) contains a buffer to store frames received from the bit stream.).

As per Claim 31, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch is arranged to perform frame-based switching** (Col. 4, lines 64-67; col. 5, lines 1-3. Data is passed through channels in frames.).

As per Claim 32, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement is provided with storage means to queue traffic at its subelements** (Figure 2; col. 11, lines 6-13. A medium access unit (21-23) contains a buffer to store frames received from the bit stream.).

As per Claim 35, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement is arranged to switch cells or packets** (Col. 22, lines 20-24. The switching arrangement can be used in a packet switching environment.).

As per Claim 36, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement includes at least one wavelength switch** (Col. 22, lines 27-38. In one possible scenario regarding the switching arrangement, a dynamic transfer mode switch may be connected to a dense wavelength division multiplexing node, on which the dynamic transfer mode switches are sent via a different wavelength.).

As per Claim 37, Bohm discloses **a switch arrangement as claimed in claim 28 wherein the ingress subelements and egress subelements are bi-directional** (Col. 21, lines 59-64. The common input/output stage contains inputs and outputs that are switched internally. This is switching within the same element.).

As per Claim 38, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the number of ingress subelements is not equal to the number of egress subelements** (Col. 10, lines 44-45. The number of switching elements does not have to be the same.).

As per Claim 40, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of ingress subelements, at least one switching stage is provided** (Col. 3, lines 15-19. The multistage switch of the invention is comprised of switching elements arranged in stages. Each element comprises a number of input ports.).

As per Claim 41, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement comprises a multi-stage switching structure,**

wherein within each aggregation of egress subelements, at least one switching stage is provided (Col. 3, lines 15-19. The multistage switch of the invention is comprised of switching elements arranged in stages. Each element comprises a number of output ports.).

As per Claim 42, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of ingress subelements, at least one time-switching stage and/or at least one spatial switching stage is provided** (Col. 3, lines 36-40. All switching elements in all stages of the invention can perform time and space switching.).

As per Claim 43, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement comprises a multi-stage switching structure, wherein within each aggregation of egress subelements, at least one time-switching stage and/or at least one spatial switching stage is provided** (Col. 3, lines 36-40. All switching elements in all stages of the invention can perform time and space switching.).

As per Claim 49, Bohm is silent on **a switch arrangement as claimed in claim 28, wherein the arrangement of one or more time-switching stages provided within each ingress aggregation of ingress subelements and/or each egress aggregation of egress subelements implements one or more of the following: the prevention of data contention at both the ingress subelements and the egress subelements of the switch arrangement;**

the correction of the sequencing of data at the egress subelements of the switch arrangement; and

the provision of contiguity of data at the egress subelements of the switch arrangement.

However, Klausmeier teaches a time division switching technique wherein the content of the buffer is read according to a read out sequence so that the information in each slot of the input frame is rearranged into the appropriate slot in the output (Col. 3, lines 11-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include the correction of sequencing data taught by Klausmeier to effectively connect multiple input and outputs (Col. 3, lines 30-32).

As per Claim 50, Bohm is silent on **a switch arrangement as claimed in claim 28, wherein at least one time-switching stage within is implemented using one or more time-slot interchangers.**

However, Klausmeier teaches a time slot interchanger (TSI) can be used to implement the interconnecting of inputs and outputs (Col. 3, lines 11-13).

Examiner maintains motivation to combine the teachings of Bohm to include the teachings of Klausmeier as disclosed in Claim 49.

As per Claim 55, Bohm discloses **a switch arrangement as claimed in claim 28, wherein the switch arrangement is arranged to implement a channel assignment process including the switching of traffic in both the space and time**

domains (Col.3, lines 10-12. An object of the invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.), **said process comprising:**

receiving traffic along a number of ingress subelements of the switch (Col. 3, lines 20-21. Incoming bit streams are received at input ports. Figure 1; col. 10, lines 12-24. Figure 1 shows three stages (105, 110, and 115) that contain nine total switching elements (120) that each contains three input ports and three output ports. These ports correspond to "subelements" of applicant's invention.);

for each ingress aggregation comprising a subset of said plurality of ingress subelements (Col. 3, lines 15-19. The multistage switch comprises a number of switching elements that are arranged in stages. Each element contains a number of input ports.), **aggregating one or more time-slots of the ingress subelements comprising said ingress aggregation to form one or more aggregated time-space channels** (Col. 8, lines 50-53. Channel data of different time slots, but pertaining to the same channel may be switched via different paths.);

assigning one or more inner time-space channels (Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to "inner time-space channels" are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements.) **available through at least**

one inner time-shared spatial switching stage of the switch arrangement to each aggregated time-space channel (Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.);

and assigning a plurality of end-to-end time-space channels from the plurality of ingress subelements to a plurality of egress subelements through the switch arrangement after said aggregated channels have been assigned through said at least one inner time-shared spatial switching stage (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage.).

As per Claim 56, Bohm discloses **a network comprising one or more switch arrangements as claimed in claim 28** (Col. 2, lines 33-45. Input ports take in data from a network and output ports send data to a network.).

As per Claim 68, Bohm teaches **a channel assignment process for a multi-stage switch arrangement having a plurality of inputs arranged in a plurality of logical associations and a plurality of outputs** (Col.3, lines 10-12. An object of the

invention is to establish multirate channels in multipath multistage switches. Col. 3, lines 19-22. Each switching element provides for time and space switching.), **wherein time-slotted traffic is received by each logical association of inputs is operated on by one or more switching stages arranged to operate only on traffic provided by the respective logical association of inputs** (Col. 3, lines 22-28. Output ports of one stage are connected to input ports of another stage. A control unit is used to control operations of the switching elements.), **the channel assignment process comprising: for each logical association, aggregating the time-slots carrying traffic from the inputs forming said logical association to form a channel comprising a plurality of logically associated time-slots** (Col. 5, lines 49-53. A bit stream is divided into recurring frames, and each of the frames is divided into time slots. Col. 7, lines 64-67, col. 8, lies 1-7. An example of time slot aggregation: A first portion of data **in at least one time** slot from an output port of the intermediate stage is sent to an input port of a last switching element.);

determining a path through a spatial switching stage of the switch arrangement arranged to receive a said channel from each of said logical associations of inputs of the switch arrangement (Col. 7, lines 40-55. Data is sent from the output port of the first stage to an input port of an intermediate stage. Data is sent from an output port of an intermediate stage to an input port of a last stage.);

and determining a path for each time-slot within each logical association such that a plurality of end-to-end time-space channels are provided for one or more inputs of the switch arrangement to their requested output via said channel

through said spatial switching stage of the switch arrangement (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to "inner time-space channels" are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.).

Bohm is silent on the aggregation of switches being arranged in a "logical" configuration.

However, Klausmeier teaches a switching element is arranged or factored logically into sub-arrays of sub-elements or switching stages (Figure 4a; Col. 3, lines 46-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include logical switching arrangements to consume less power and occupy less space (Col. 6, lines 9-14).

As per Claim 69, Bohm discloses **a channel assignment process as claimed in claim 68, wherein the outputs of the switch arrangement are logically associated with one or more switching stages** (Col. 3, lines 22-28. Output ports of one stage are connected to input ports of another stage. A control unit is used to control operations of the switching elements.), **and said step of determining a path for each time-slot within each logical association further comprising determining a path within each logical association of the outputs of the switch arrangement such that said plurality of end-to-end time-space channels are provided** (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the

last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.).

Bohm is silent on the aggregation of switches being arranged in a "logical" configuration.

However, Klausmeier teaches a switching element is arranged or factored logically into sub-arrays of sub-elements or switching stages (Figure 4a; Col. 3, lines 46-56).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include logical switching arrangements to consume less power and occupy less space (Col. 6, lines 9-14).

11. Claims 44-48 and 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohm and Klausmeier, and further in view of US Patent Publication 2002/0001305 A1 by Hughes et al (hereinafter "Hughes").

As per Claim 44, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 28, wherein the switch arrangement comprises a multi-stage switching structure, wherein within at least one ingress aggregation of ingress subelements, a first time-switching stage; a spatial switching stage; and a second time-switching stage are provided.**

However, Hughes teaches a time-space-time switching fabric that contains a plurality of ingress ports and a plurality of egress ports (Abstract). Further, Figure 5 shows 3-stage switching of the invention. Each TSE stage (transition switching element) contains a 3-stage time-space-time-fabric ([0061]). Each ingress serial link feeds an ingress time stage, and then feeds a space switch.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include a time-space-time configuration of each stage taught by Hughes to achieve a desired switching capacity that is larger than a single space switching stage ([0015]).

As per Claim 45, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 28, wherein the switch arrangement comprises a multi-stage switching structure, wherein within at least one aggregation of egress subelements, a first time- switching stage; a spatial switching stage; and a second time-switching stage are provided.**

However, Hughes teaches a time-space-time switching fabric that contains a plurality of ingress ports and a plurality of egress ports (Abstract). Further, Figure 5 shows 3-stage switching of the invention. Each TSE stage (transition switching element) contains a 3-stage time-space-time-fabric ([0061]). Each egress time stage feeds a time-space-time flow to the egress ports.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include a time-

space-time configuration of each stage taught by Hughes to achieve a desired switching capacity that is larger than a single space switching stage ([0015]).

As per Claim 46, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 28, wherein at least one inner spatial switching stage of the switch arrangement comprises one or more space switches which are shared in time between the ingress and egress aggregation elements.**

However, Hughes teaches that each TSE contains 3 stages internally: a time switching stage, a space switching stage, and a last time switching stage ([0061]). In Figure 5, the multi-stage switching arrangement contains three columns of TSEs, each column represents a stage. The first column is the first stage, the second column is the middle stage, and the last column is the final stage ([0093]). The switching fabric of the design allows the 3-stage fabric to have a depth of 2 or more TSEs, thus allowing multiple space switches in the middle switching stage ([0087]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include a time-space-time configuration of each stage taught by Hughes to achieve a desired switching capacity that is larger than a single space switching stage ([0015]).

As per Claim 47, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 46, wherein traffic is logically switched by the switch arrangement firstly in a time-switching stage within an aggregation element, secondly by a spatial switching stage within an aggregation element, thirdly by a time-switching stage within an aggregation element, fourthly by a time-shared**

spatial switching stage of the switch arrangement, fifthly in a time-switching stage within an aggregation element, sixthly by a spatial switching stage within an aggregation element, and finally by a time-switching stage within an aggregation element.

However, Hughes teaches this configuration, as an alternating time-space-time-space-time-space-time fabric arrangement ([0017]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include the switching arrangement T-S-T-S-T-S-T taught by Hughes to allow for simpler routing algorithms ([0017]).

As per Claim 48, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 47, wherein the switch arrangement comprises a plurality of switching stages forming a permutation of said seven time and spatial switching stages.**

However, Hughes teaches that each time-space-time fabric can implement arbitrary S! permutations ([0014]).

Examiner maintains motivation to combine the teachings of Bohm and Klausmeier to include the teachings of Hughes as disclosed in Claim 47.

As per Claim 57, Bohm and Klausmeier are silent on **a suite of one or more computer programs arranged to implement the channel assignment process according to claim 1.**

However, Hughes teaches the process of the invention can be included in software applications ([0071]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include implementing software taught by Hughes to save space in the memory stages ([0071]).

As per Claim 58, Bohm and Klausmeier are silent on **a suite of at least one computer programs arranged to implement the scheduling process according to claim 24.**

However, Hughes teaches the process of the invention can be included in software applications ([0071]).

Examiner maintains motivation to combine the teachings of Bohm and Klausmeier to include the teachings of Hughes as disclosed in Claim 57.

As per Claim 59, Bohm and Klausmeier are silent on **a suite of one or more computer programs arranged to implement the scheduling process according to claim 26.**

However, Hughes teaches the process of the invention can be included in software applications ([0071]).

Examiner maintains motivation to combine the teachings of Bohm and Klausmeier to include the teachings of Hughes as disclosed in Claim 57.

As per Claim 60, Bohm and Klausmeier are silent on **a suite of at least one computer programs as claimed in claim 57, at least partly arranged to be implemented in hardware.**

However, Hughes teaches TSEs use multiplexors and flip flops in the construction of the switching circuit ([0126]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include hardware taught by Hughes to efficiently implement the small amount of memory required ([0126]).

12. Claims 10-14 rejected under 35 U.S.C. 103(a) as being unpatentable over Bohm and Klausmeier and further in view of US Patent Publication 2003/0202545 A1 by Arbel et al (hereinafter "Arbel").

As per Claim 10, Bohm discloses **a channel assignment process as claimed in claim 1, in which the step of assigning inner time-space channels available through at least one inner time-shared spatial switching stage of the switch arrangement to said plurality of aggregated time-space channels is implemented using N processors, where N is the number of aggregations of ingress or egress elements of the switch arrangement** (Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-

38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.).

Bohm and Klausmeier are silent in regards to assigning the channels using processors.

However, Arbel teaches a switching network with multiple stages (Abstract) that processes the data flow between inputs and outputs via parallel processors ([0026]. Input processors are used to transfer data from the input ports.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include processors taught by Arbel, to help facilitate the reduction of processing speed.

As per Claim 11, Bohm in view of Arbel discloses **a channel assignment process as claimed in claim 1, wherein each ingress subelement of the switch arrangement is associated with a plurality of processors arranged to operate in parallel, with each other, each processor finding a number of available channels between an ingress subelement and a switch in the final switching stage of an**

ingress aggregation (Bohm; Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage. Arbel; [0026]. Input processors are used to transfer data from the input ports. The switching arrangement processes data flow between inputs and outputs via parallel processors.), **wherein the channels within the ingress aggregation element are found by sequential inspection of the status of channels within the ingress aggregation element**.

Bohm is silent on sequential inspection of the channels.

However, Arbel teaches the process for establishing channels continues sequentially until all stages are using a particular path. [0070]. Multiple paths may be chosen as well.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm to include sequential inspection of channels taught by Arbel to decrease the loss of data ([0070]).

As per Claim 12, Bohm in view of Arbel discloses **a channel assignment process as claimed in claim 1, wherein each egress subelement of the switch arrangement is associated with a plurality of processors arranged to operate in parallel with each other, each processor finding a number of available channels between a switch in the first switching stage of an egress aggregation and an egress subelement of the switch arrangement** (Bohm; Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the

intermediate switching elements connected to the input ports of the last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage. Arbel; [0026]. Input processors are used to transfer data from the input ports. The switching arrangement processes data flow between inputs and outputs via parallel processors.), **wherein the channels within the egress aggregation element are found by sequential inspection of the status of channels within the egress aggregation element** (Arbel; [0069]. The process for establishing channels continues sequentially until all stages are using a particular path. [0070]. Multiple paths may be chosen as well.).

Examiner maintains motivation to combine the teachings of Bohm to include the teachings of Arbel as disclosed in Claim 11.

As per Claim 13, Bohm in view of Arbel discloses **a channel assignment process as claimed in claim 1** (Bohm; Abstract), **wherein each ingress aggregation of the switch arrangement is provided with one or more processors arranged to operate in parallel with the processors of the other ingress aggregations of the switch arrangement** (Arbel; [0026]. Input processors are used to transfer data from the input ports. The switching arrangement processes data flow between inputs and outputs via parallel processors.), **each processor finding the required number of available aggregated channels between an ingress aggregation and an egress aggregation via the a switch in the final switching stage of an ingress aggregation** (Bohm; Col.

5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.), **wherein the channels are found by sequential inspection** (Arbel; [0069]. The process for establishing channels continues sequentially until all stages are using a particular path. [0070]. Multiple paths may be chosen as well.).

Examiner maintains motivation to combine the teachings of Bohm to include the teachings of Arbel as disclosed in Claim 11.

As per Claim 14, Bohm in view of Arbel discloses **a channel assignment process as claimed in claim 1** (Bohm; Abstract), **wherein each ingress aggregation of the switch arrangement is associated with a plurality of processors arranged to**

operate in parallel with each other (Arbel; [0026]. Input processors are used to transfer data from the input ports. The switching arrangement processes data flow between inputs and outputs via parallel processors.), **each processor finding a number of available aggregated channels between an ingress aggregation and an egress aggregation via the inner time-shared spatial switching stage of the switch arrangement** (Bohm; Col. 5, lines 18-23. There are multiple paths established between output ports and input ports of more than one switching element. Figure 1 also shows the plurality of switching elements, each of which contain pluralities of inputs and outputs. The lines showing connections are first connected at the output of stage 1 (105) to inputs of intermediate stage 2 (110). From the outputs of the intermediate stage, a connection is made at the inputs of the last stage. Col. 7, lines 27-38. The method comprises a switching apparatus that contains a first set of switching elements, an intermediate set of switching elements, and a last set of switching elements. Channel connections relating to “inner time-space channels” are the connections between the output ports of the first set of switching elements and the input ports of the intermediate switching elements, as well as the output ports of the intermediate switching elements connected to the input ports of the last switching elements. Col. 18, lines 3-13; Figure 1 and 6. The intermediate switching stage is capable of performing time switching and space switching. A channel is created for the bit stream between the first and the last stage via the intermediate stage.), **wherein the channels are found by sequential inspection of the status of channels from the ingress aggregation and to the egress aggregation** (Arbel; [0069]. The process for establishing channels continues

sequentially until all stages are using a particular path. [0070]. Multiple paths may be chosen as well.).

Examiner maintains motivation to combine the teachings of Bohm to include the teachings of Arbel as disclosed in Claim 11.

13. Claims 33, 34, and 51-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bohm and Klausmeier, and further in view of US Patent Publication 2003/0021266 A1 by Oki et al (hereinafter "Oki").

As per Claim 33, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 32, wherein said storage means is implemented using virtual output queuing.**

However, Oki teaches a method of cell scheduling using a matching algorithm that incorporates virtual output queuing (VOQ) ([0051]. VOQs receive from inputs and are associated with corresponding outputs.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include virtual output queuing taught by Oki to eliminate problems caused by head of line blocking ([0051]).

As per Claim 34, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 33, wherein the virtual output queues are implemented in random access memory.**

However, Oki teaches memory can be used to buffer cells at the virtual output queues ([0101].

Examiner motivation to combine the teachings of Bohm and Klausmeier wit the teachings of Oki as disclosed in Claim 33.

As per Claim 51, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 28, wherein at least one time-switching stage within an ingress aggregation is implemented using one or more virtual output queues implemented in random access memory.**

However, Oki teaches memory can be used to buffer cells at the virtual output queues ([0101].

Examiner motivation to combine the teachings of Bohm and Klausmeier wit the teachings of Oki as disclosed in Claim 33.

As per Claim 52, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 28, wherein the switch arrangement includes parallel processor means arranged to assign said plurality of aggregated time-space channels in parallel to said logical inner channels through the switch arrangement.**

However, Oki teaches most of the scheduler operations are controlled by a microprocessor ([0214].). Separate instances of the main scheduler timing-controlled

operations can be run in parallel ([0185]). A sub-scheduler element of the invention is set to “1” if certain conditions are met.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include parallel processing taught by Oki to eliminate problems caused by head of line blocking ([0051]).

As per Claim 53, Bohm and Klausmeier are silent on **a switch arrangement as claimed in claim 28, wherein the switch arrangement includes parallel processor means arranged to assign a plurality of time-space channels in parallel to said logical inner channels through an ingress and/or egress aggregation.**

However, Oki teaches most of the scheduler operations are controlled by a microprocessor ([0214].). Separate instances of the main scheduler timing-controlled operations can be run in parallel ([0185]). A sub-scheduler element of the invention is set to “1” if certain conditions are met.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of Bohm and Klausmeier to include parallel processing taught by Oki to eliminate problems caused by head of line blocking ([0051]).

Allowable Subject Matter

14. Claims 15-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Prior art made of record, but not relied upon include:

US Patent 6,876,649 B1 by Beshai discloses a high-capacity wavelength and time-division multiplexed switch.

US Patent 6,643,293 B1 by Carr et al discloses shaping ATM traffic using virtual channel connections.

US Patent Publication 2002/0039364 A1 by Kamiya et al discloses a scheduler of a crosspoint switch.

US patent Publication 2003/0133452 A1 by Su discloses a multi-channel data transmission control method.

US Patent 7,027,436 B2 by Ryan et al discloses a communication multi-stage switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN ELLIOTT whose telephone number is (571)270-7163. The examiner can normally be reached on Monday thru Thursday, 5:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Taghi Arani can be reached on 1-571-272-3787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/B. E./
Examiner, Art Unit 4144

/Taghi T. Arani/

Supervisory Patent Examiner, Art Unit 4144